TMOS FET Transistor

N–Channel — Enhancement

3 DRAIN

2 GATE
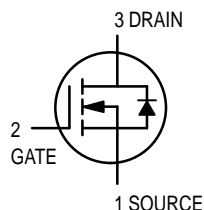
1 SOURCE

2N7000

Motorola Preferred Device
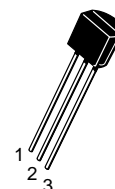
CASE 29–04, STYLE 22
TO–92 (TO–226AA)

1
2
3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–repetitive (t_p ≤ 50 µs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	I_D I_{DM}	200 500	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	357	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 10 µAdc)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 Vdc, V_{GS} = 0) (V_{DS} = 48 Vdc, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	1.0 1.0	µAdc mAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	−10	nAdc
ON CHARACTERISTICS[1]				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc)	$V_{GS(th)}$	0.8	3.0	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 75 mAdc)	$r_{DS(on)}$	— —	5.0 6.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 0.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 75 mAdc)	$V_{DS(on)}$	— —	2.5 0.45	Vdc

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS[1] **(continued)**					
On–State Drain Current (V_{GS} = 4.5 Vdc, V_{DS} = 10 Vdc)		$I_{d(on)}$	75	—	mAdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 200 mAdc)		g_{fs}	100	—	μmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5.0	
SWITCHING CHARACTERISTICS[1]					
Turn–On Delay Time	(V_{DD} = 15 V, I_D = 500 mA, R_{gen} = 25 ohms, R_L = 25 ohms)	t_{on}	—	10	ns
Turn–Off Delay Time		t_{off}	—	10	

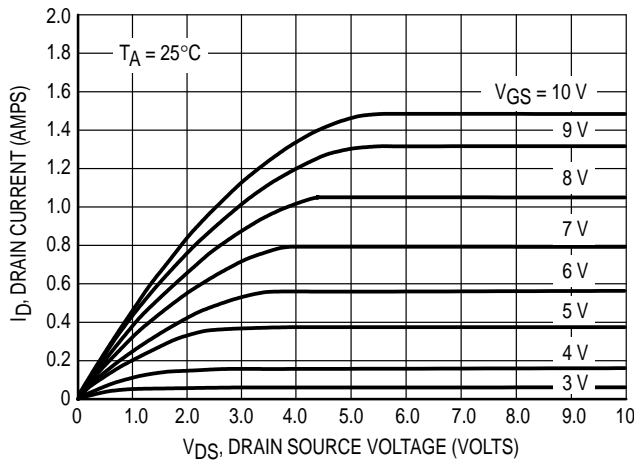1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
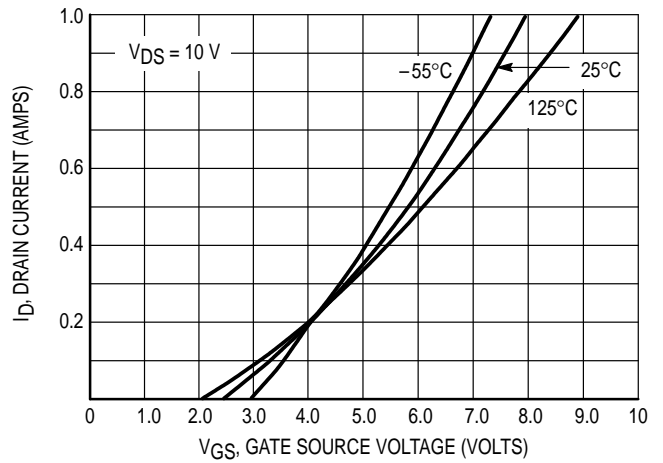

Figure 1. Ohmic Region
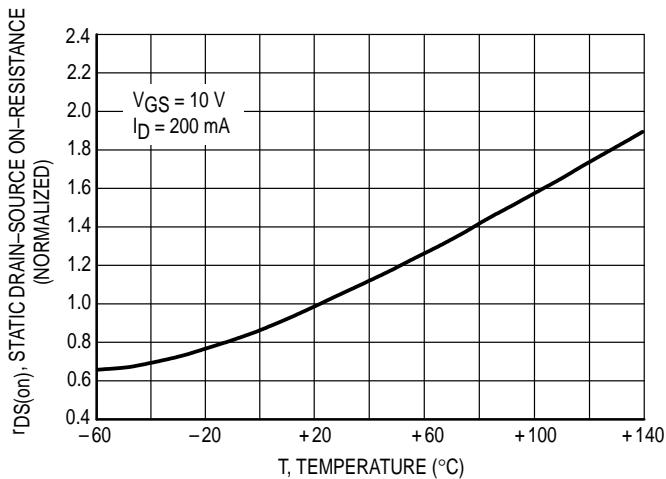

Figure 2. Transfer Characteristics

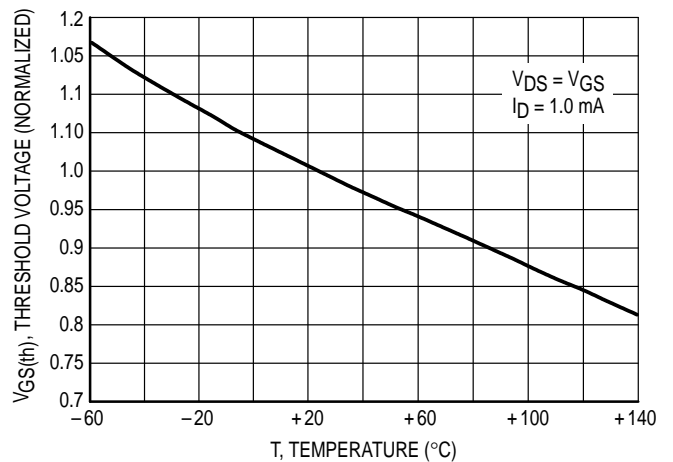Figure 3. Temperature versus Static
Drain–Source On–Resistance

Figure 4. Temperature versus Gate
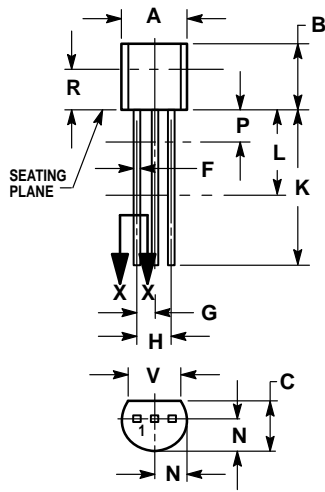Threshold Voltage

PACKAGE DIMENSIONS

SEATING PLANE

SECTION X–X

CASE 029–04
(TO–226AA)
ISSUE AD
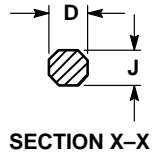
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

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